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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,391	07/11/2003	Tamio Ikehashi	240192US2	3324

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EXAMINER	
TRAN, MICHAEL THANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,391	IKEHASHI, TAMIO	
	Examiner	Art Unit	
	Michael t Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 11, 2003 through November 10, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14* is/are rejected.

7)☒ Claim(s) *2-13,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *101003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated July 11, 2003 through November 10, 2003, claims 1-16 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed October 10, 2003 has been considered.

Claim Objections

4. Claims 2-13, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claim 1 is rejected under 35 U.S.C 102(b) as being anticipated by Kanbara [U.S. Patent #5,036,231].

With respect to claim 1, Kanbara discloses a semiconductor memory device comprising: a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate [see column 1, lines 10-20 – in the cited section, Kanbara states that there are related cases with regard to the disclosed invention. The related cases [U.S. Patent 5,060,034; and 5,079,606] disclose the substrate structure]; a memory cell array having a plurality of memory cells formed and arranged on said semiconductor layer of said device substrate, each said memory cell having a MOS transistor structure with a body in an electrically floating state to store data based on a majority carrier accumulation state of said body [see column 1, lines 10-20]; and a sense amplifier circuit configured to performed data read out of said memory cell array, said sense amplifier circuit including a bipolar transistor for performing current amplification of a memory cell selected during data reading [see column 1, lines 20-35].

Claim Rejections – 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbara [U.S. Patent # 5,036,231] in view of Wiedmann et al. [U.S. Patent # 5,453,949].

Kanbara discloses a semiconductor memory device comprising: a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate [see column 1, lines 10-20 – in the cited section, Kanbara states that there are related cases with regard to the disclosed invention. The related cases [U.S. Patent 5,060,034; and 5,079,606] disclose the substrate structure]; a memory cell array having a plurality of memory cells formed and arranged on said semiconductor layer of said device substrate, each said memory cell having a MOS transistor structure with a body in an electrically floating state to store data based on a majority carrier accumulation state of said body [see column 1, lines 10-20]; and a sense amplifier circuit configured to performed data read out of said memory cell array, said sense amplifier circuit including a bipolar transistor for performing current amplification of a memory cell selected during data reading [see column 1, lines 20-35].

Kanbara discloses all of the above mentioned but is silent about the fact that the memory contain a wordline driver arranged by using a bipolar transistor. However, Wiedmann et al. disclose, in column 4, lines 15-25 that it is well known and necessary for a memory device to have a wordline driver in order to facilitate data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Kanbara memory circuit element to include a wordline driver as taught by Wiedmann et al., since Wiedmann et al. show that it is well known and advantageous in the art to provide a memory circuit element with a wordline driver arranged by using a bipolar transistor in order to drive the large capacitance of the word lines [see column 4, lines 15-25].

Allowable Subject Matter

9. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Said sense amplifier circuit has a pre-sense amplifier including said bipolar transistor and a main sense amplifier for amplification of an output of said pre-sense amplifier.
- Said word-line driver has a pull-up lateral transistor and a pull-down lateral transistor which are formed at said semiconductor layer of said device substrate.

Conclusion

10. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

12. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2818
August 6, 2004